FET UPCONVERTER DESIGN USING LOAD DEPENDENT MIXING TRANSCONDUCTANCE

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ABSTRACT

A novel FET upconverter design procedure using load dependent mixing transconductance in the FET equivalent circuit has been developed. It optimizes the drain network for acceptable match at the selected sideband and desired LO rejection while avoiding impedance values in the LO frequency range which would otherwise cause severe degradation in conversion loss.

INTRODUCTION

A good deal of research has been conducted on the use of GaAs MESFETs in frequency conversion circuits such as mixers and multipliers. Much of this effort concentrated on conversion efficiency dependence on bias, input LO power, and in some cases, terminating impedances at both ports for the various signal frequencies. For mixers, apart from the obvious input and output matching requirements, the general consensus is that only terminations at IF, RF, image (possibly), and LO frequencies need to be considered. For a gate downconverter, the trend is to short-circuit the IF at the gate and the RF and LO at the drain. Yet, given the major influence of the LO, the importance of its drain termination appears to have been somewhat underestimated. Since Harrop & Claasen's work identified the optimal LO impedance to be a short-circuit (1), little detailed supporting evidence for that particular result has been offered. More recently, Maas (2) justified that choice by stating that a "well-behaved" FET transconductance mixer should always operate in the current saturation region with the smallest LO drain voltage variation.

To design a FET mixer circuit, the frequency behavior of the embedding networks thus requires careful analysis. At the input, the combining circuit must offer good match and signal isolation. At the output, the network synthesis must account for the matching of the selected sideband and a desired LO rejection. Both circuits must also provide optimum terminations for the other signals. For downconverters, where the IF and LO are quite far apart, the LO short-circuit at the drain appears to be a satisfactory and easily realizable approximation of optimum LO loading. For upconverters, the same conclusions should apply, but the network synthesis faces an additional problem.

The usual proximity of the RF and LO frequencies makes a simultaneous realization of the above three requirements difficult, especially over a substantial LO/RF bandwidth. Furthermore, the authors' experience with FET upconverter measurements over a range of RFs from 1 to 7 GHz revealed that the optimum LO loading at the drain is dependent on FET parameters and operating frequency and thus not always identical to a short-circuit. In general, the conversion gain was fairly flat and LO-termination insensitive around the optimum impedance while a sharp dip of up to 20 dB occurred over a narrow range of impedance values. Therefore, avoiding the minimum region rather than maximizing gain should be the goal sought when designing FET mixers.

It is the aim of this work to contribute to more accurate MESFET upconverter design by thoroughly investigating the LO loading phenomenon and integrating the results into a design method. The approach taken relies on a combination of RF measurements and equivalent circuit representations with a frequency domain CAD tool such as Touchstone to create a simple but realistic mixer model simulating the LO dynamic loading, thereby allowing real-time circuit analysis and synthesis.

DESCRIPTION OF THE METHOD

We are considering an upconverter with both LO and IF fed to the gate from a broadband 50 Ohm source. The proposed design method contains the following steps:

a. With the drain terminated in a broadband 50 Ohm load, find the bias and the input LO power which yield the "optimum" operation of the FET; here, optimum means that both conversion gain and third-order intercept point (IP3) are maximized while the output level of the second and third LO harmonics is kept as low as possible, thus aiming at relaxing the mixer's sensitivity to uncontrollable impedances so as to isolate the effects of the LO termination at the drain.

b. Use a simple load-pull method to vary the drain reflection coefficient at the LO frequency while keeping a good 50 Ohm at the chosen sideband (RF) and measure conversion gain over the LO frequency range; the drain IF load is fixed as a

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short-circuit. This renders conversion gain C_g as a function of the LO reflection coefficient Γ and the LO frequency f_{LO} :

$$C_g = C_g\,(\Gamma, f_{LO}) \qquad [1]$$

c. Construct three equivalent circuits representing the FET at IF, RF, and LO; find their element values with a standard least-square optimization method from S parameters measured at the LO level obtained in a).

d. Assume the transconductance is the sole nonlinear element of the FET. In the RF equivalent circuit, define a conversion current source, to be controlled by the IF gate voltage, with an associated "mixing transconductance" g_m. It must obviously be a function of Γ and f_{LO} :

$$g_m = g_m\,(\Gamma, f_{LO}) \qquad [2]$$

e. Use the IF and RF equivalent circuits to determine the theoretical S_{21} from IF to RF. First, the IF gate voltage is calculated over the desired bandwidth while the drain is loaded with its actual termination; next, calculating the current of the conversion source, the theoretical S_{21} is determined as a function of g_m and sideband frequency f_s . By definition, this S_{21} must be equal to the measured conversion gain C_g :

$$S_{21}\,(g_m, f_s) \equiv C_g\,(\Gamma, f_{LO}) \qquad [3]$$

with f_s and f_{LO} related by the IF frequency used. The solution of this equation for g_m allows the extraction of [2].

f. Study the LO circuit with a model of the experimental load of b). Voltage patterns are created on each element as the load variables are changed. This yields functions of the type:

$$V_{LOi} = V_{LOi}(\Gamma, f_{LO}) \qquad [4]$$

Then, key elements can be selected by correlating [1] and [4].

g. Assume that the g_m variations are caused by a mechanism linking g_m to the LO voltages of f) on a few key elements. Then, g_m can be written as:

$$g_m = g_m(V_{LO1}, V_{LO2}, \cdots) \qquad [5]$$

Using least-square curve fitting, solve for [5] by combining [2] and [4] with the minimum number of LO voltage variables.

The above formulation in effect couples internal parameters and voltages of the transistor to yield the same type of expression commonly found in FET models; this formulation is expected to be more universal than if g_m was related only to the external circuit as in [2]. Practically, a significant computation economy can also be achieved since the LO voltage variables are implicitly functions of frequency.

h. Upconverter performance optimization can now be performed as the effect of the chosen output matching circuit on the selected LO voltages can be evaluated, and in turn the mixing transconductance and conversion gain predicted.

We thus have an upconverter representation comprised of three interconnected equivalent circuits featuring an LO-load dependent mixing transconductance in the RF equivalent circuit. The method is a version of the classical mixer theory with both large-signal and small-signal solutions featured. The conversion matrix is represented by the three circuits lumped together; important signal interactions can be visualized to support some of our assumptions (e.g. concerning the second harmonic effects).

In the process of isolating the LO reflection effect, step a) is important to achieve the goals of predictability and repeatability, because a method based on the careful characterization of the LO reflection mechanisms will be useful only if the latter remains the dominant factor in affecting conversion gain.

The large-signal S parameters technique for the pumping solution has limitations in accuracy, but its use is necessary to keep the measurement and analysis procedure simple. Besides, the good accuracy we have obtained suggests that the deviations are not very significant.

Neglecting reactive nonlinearities (their contribution having been judged insignificant by many researchers) together with nulling the channel conductance contribution by short-circuiting the IF, effectively make our upconverter a transconductance mixer as assumed in step d) above.

RESULTS

An NE70083 (L_g = 0.5 um) was chosen for the characterization. 0 dBm LO power and V_{gg} = -.33 V, V_{dd} = 3.0 V, yielded the optimum conversion characteristics. The low LO power allows ease of measurements and better accuracy under the model's assumptions. Typically, a 2 dB conversion loss and a 6 dBm IP3 were obtained at 1.52 GHz; the degradation from the maximum conversion bias values at that LO power was 3 and 2 dB, respectively. Figure 1 shows a typical conversion gain LO-loading dependency. Note the sharp dip (-13 dB) and the flat maximum (0.5 dB), somewhat off the short-circuit point. This plot corroborates fairly well the results of (3). Using the LO reflection circuit (Fig. 2), the measured conversion gain could be compared with voltage patterns across certain elements. Not surprisingly, V_{cgs} and V_{rds} (Fig. 3) were observed to correlate well with the conversion gain patterns. An expression relating these two voltages to the mixing transconductance was found such that when the RF equivalent circuit (Fig. 4) employing this "LO voltage dependent" transconductance was used, the computed conversion agreed well with the measured data (Fig. 5).

The measured minimum and maximum conversion gain impedances were deduced to correspond to parallel and series resonance at the drain of the FET. Internal feedback

appears to play an important role, especially as the operating frequency is increased. Therefore, our results reinforce the findings of Rauscher (4) in showing that the feedback and resonances at the LO frequency, caused by the transistor's internal elements and package parasitics, directly influence the conversion gain behaviour.

Obviously, the physics behind the conversion extrema is not readily available from the model. However, the phenomenon of drain-voltage induced pinch-off voltage shifts, observed in the DC characteristics of our FET and described by (5,6,7), may very well explain why parallel resonance at the drain hinders conversion efficiency. Neglecting transit-time effects at "low" frequencies, it is when the increase in the pinch-off voltage range is largest and when the two controlling voltages (V_{cgs} & V_{rds}) are out of phase that the most severe conversion degradation should occur. Using the LO circuit, we calculate that these two conditions actually happen simultaneously at parallel resonance. At the other extreme, the series resonance corresponds to the case of minimum transconductance modulation by the drain voltage. Furthermore, the study of the voltage patterns of the LO circuit at higher frequencies reveals that the short-circuit approximation to optimum LO loading becomes progressively more inaccurate. For instance, short-circuiting the LO at 10 GHz for the transistor studied here would seriously degrade the mixer performance.

CONCLUSION

Our procedure thus allows simulations of the conversion gain over a specific bandwidth using a few microwave measurements and simple equivalent circuits, instead of the common quasi-static approach where the FET DC characteristics are used to calculate mixing products, as in (5). Our method is less versatile but should yield optimal accuracy within its range of applicability; furthermore, it is more suitable than harmonic balance-based models as a tool for practical design. Using the concept of LO-load dependent mixing transconductance, a CAD tool such as Touchstone can serve to simulate conversion gain with any particular network at the drain and allow optimization of its parameters to obtain desired flatness, gain, and LO rejection over the complete bandwidth. The model will be most useful for monolithic implementations lacking tuning capabilities.

From a more general point of view, this work has demonstrated the acute importance of the LO drain termination of a gate mixer in determining conversion efficiency. It has been shown that neither the short- nor the open-circuit drain termination at the LO frequency will cause conversion gain extrema. The results should apply to downconverters as well, since the same first-order mixing process is involved.

ACKNOWLEDGEMENTS

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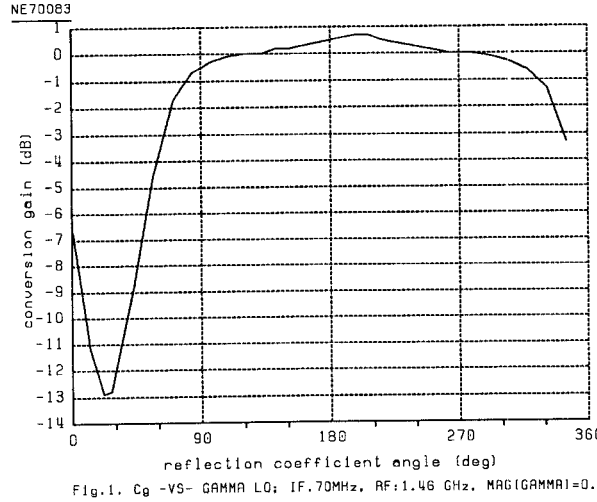

Fig.1. C_8 -VS- GAMMA LO; IF:70MHz, RF:1.46 GHz, MAG(GAMMA)=0.8

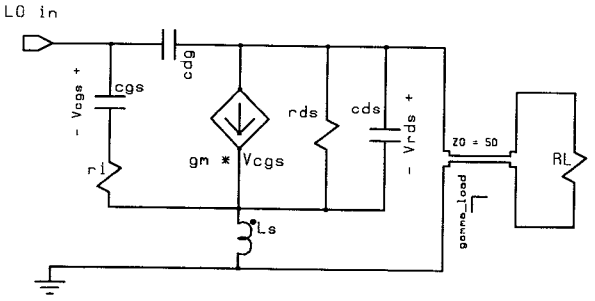

Fig.2: LO equivalent circuit with reflection load

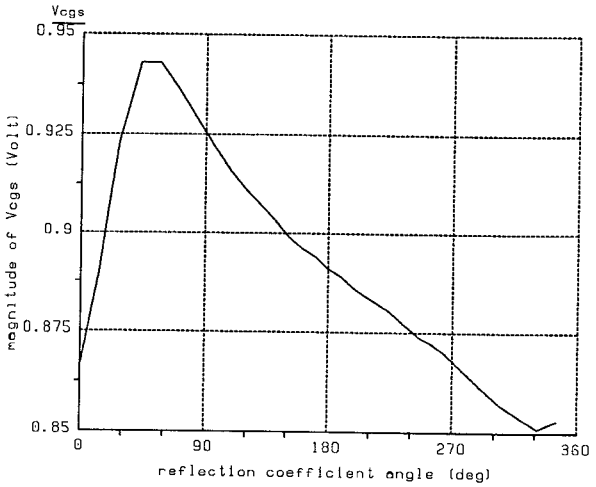

Fig.3a: MAGNITUDE OF VCGS -VS- GAMMA LO; RF:1.46 GHz

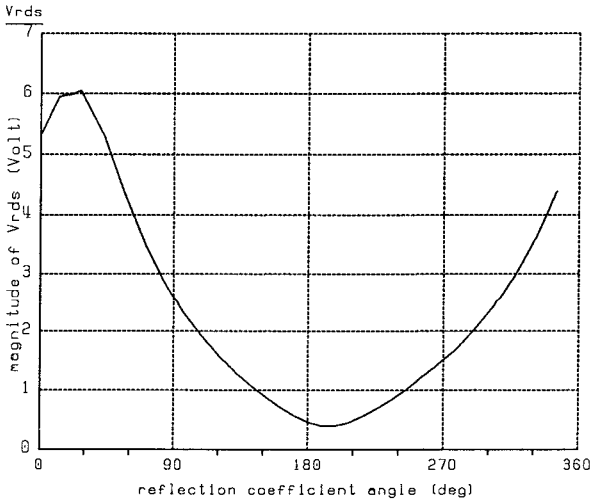

Fig.3b: MAGNITUDE OF VRDS -VS- GAMMA LO, RF:1.46 GHz, MAG(GAMMA)=0.8

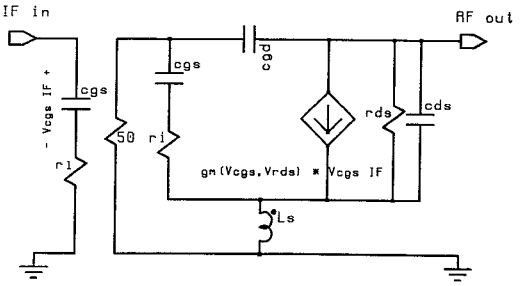

Fig.4: Sideband equivalent circuit

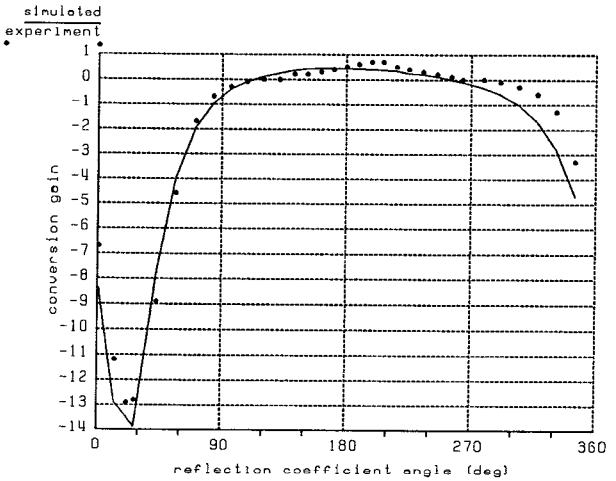

Fig.5: EXPERIMENTAL AND SIMULATED Cg -VS- GAMMA LO, RF:1.46 GHz, MAG(GAMMA)=0.8